CLAIMS

What is claimed is:

1. A method for expanding addressing capability of a plurality of registers connected to an interface comprising:

designating at least two of the plurality of registers as a block of registers;

providing a plurality of such blocks of registers;

designating a first register within the plurality of registers that is separate from the blocks of registers as a location register for selectively characterizing at least one of such blocks of registers as an indicated block of registers; and

designating a second register within the plurality of registers that is separate from the blocks of registers as a control register for specifying at least one operation for the indicated block of registers.

2. A method according to Claim 1, wherein the first register includes a block selector for selectively characterizing at least one of such blocks of registers as an indicated block of registers.

3. A method according to Claim 1, wherein the second register includes an operational code.

4. A method according to Claim 3, wherein the second register includes a port indicator.

5. A method according to Claim 1, wherein said first register comprises a pointer to a plurality of location registers, each indicating a register block and wherein said second register comprises a pointer to a plurality of control registers,

each control register comprising an operational code, and wherein said plurality of location registers are associated with said plurality of control registers such that a first operational code is associated with a first block and a second operational code is associated with a second block.

6. A method according to Claim 1, wherein said location and control registers comprise registers compatible with IEEE standard 802.3 clause 22.

7. A system for expanding the addressing capability of a plurality of registers, the system comprising:

a plurality of blocks of registers, each block of registers having at least two registers;

a location register separate from the plurality of blocks of registers for selectively characterizing at least one of the blocks of registers as a specified block of registers;

a control register separate from the plurality of blocks of registers for selecting at least one operational code for the specified block of registers and specifying at least one port number for the specified block of registers; and

a control engine operable to access the operational code for the specified block of registers and act on the specified block of registers at each of the specified port numbers in accordance with the operational code.

8. A system according to Claim 7, wherein the operational code specifies an operation to be performed on the specified block of registers.

9. A system according to Claim 8, wherein the operation is restricting the specified block of registers to read operations only.

10. A system according to Claim 7, wherein the operational code specifies control sequencing information.

11. A system according to Claim 10, wherein the control sequencing information instructs the control engine to proceed to a next block after completing operations with the specified block.

12. A system according to Claim 7, wherein said location register includes a block selector indicating said block.

13. A system according to Claim 7, wherein said location register includes a pointer to a block selector.

14. A system according to Claim 7, wherein said location register includes a pointer to a plurality of registers, each including a block selector.

15. A system according to Claim 7, wherein said control register is operable to store an operational code.

16. A system according to Claim 15, wherein said control register is further operable to store a register indicator indicative of a register within said block.

17. A system according to Claim 15, wherein said control register is further operable to store a port indicator.

18. A system according to Claim 7, wherein said control register is operable to specify a plurality of ports.

19. A system according to Claim 7, wherein said control register includes a pointer to a plurality of third registers, each having an operational code.

20. A system according to Claim 7, wherein said location register includes a pointer to a plurality of location registers, each indicating a register block and wherein said control register includes a pointer to a plurality of control registers, each control register storing an operational code, and wherein said plurality of block indicator registers are associated with said plurality of control registers such that a first operational code is associated with a first block and a second operational code is associated with a second block.

21. A system according to Claim 7, wherein said at least one operation is selected from the group of operations consisting of pointer handling and stream looping.

22. A system according to Claim 7, wherein said lcoation and control registers are registers specified by IEEE standard 802.3 clause 22.

23. A system according to Claim 7, further comprising:

a plurality of register banks, each bank including a plurality of register blocks.

24. A system according to Claim 23, wherein said location register further indicates at least one of said register blocks.

25. A system according to Claim 7 further comprising:

a mask register following the location register and specifying a mask for the specified block of registers.